CBCS SCHEME

USN | | | | | | | | | | |

15MT36

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Computer Organization

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Discuss with block diagram basic functional units of a computer. **(08 Marks)**

b. Explain two ways that byte address can be assigned across word. **(08 Marks)**

OR

2 a. Describe the processor clock and performance equation with respect to performance of a computer. **(08 Marks)**

b. Explain branching concept by considering example of adding 'n' numbers using straight line program and using loop. **(08 Marks)**

Module-2

3 a. Explain with example the following addressing modes:
i) Indirect mode ii) Indexing mode iii) Absolute mode. **(08 Marks)**

b. Explain shift and rotate instruction with example. **(08 Marks)**

OR

4 a. Explain the format of IEEE standard for floating point number. Also explain how normalization in IEEE is carried out. **(08 Marks)**

b. Discuss the following in case of subroutine:
i) Subroutine nesting ii) Parameter passing. **(08 Marks)**

Module-3

5 a. Discuss bus arbitration in case of DMA with schematic. **(08 Marks)**

b. Make use of timing diagram explain input data transfer using handshake scheme. **(08 Marks)**

OR

6 a. Summarize the function of I/O interface. **(05 Marks)**

b. Explain PCI bus with neat block diagram. **(05 Marks)**

c. List the sequence of events when the processor sends a command to the SCSI controller. **(06 Marks)**

Module-4

7 a. Discuss different mapping functions in case of cache. **(08 Marks)**

b. Explain SDRAM with the help of neat block diagram. **(08 Marks)**

OR

8 a. Discuss internal organization of 2M × 8 dynamic memory chips. **(05 Marks)**

b. Explain the memory hierarchy with neat diagram. **(05 Marks)**

c. Briefly discuss virtual memory organization. **(06 Marks)**

Module-5

9 a. List the control sequence for execution of Add (R3), R1 instruction. **(07 Marks)**

b. Explain with neat block diagram single-bus organization of the data path inside a processor. **(09 Marks)**

OR

10 a. Discuss microinstruction sequencing organization in micro programmed control unit. **(06 Marks)**

b. Explain with neat sketch Hardwired control unit organization. **(06 Marks)**

c. List the action needed to execute the instruction MOV (R1), R2. **(04 Marks)**

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