CBCS SCHEME

USN | | | | | | | | | | |

15MT36

Third Semester B.E. Degree Examination, June/July 2018
Computer Organization

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Draw the diagram that shows the connections between the processor and the memory. Explain the basic operational concept with an example. **(08 Marks)**

b. Perform the following arithmetic operations using 5-bit 2's complement number system (i) A + B (ii) A – B (iii) –A + B (iv) –A – B where A = –7 and B = 12. State whether result is correct or incorrect. **(08 Marks)**

OR

2 a. Write the basic performance equation and explain how each parameter is responsible for the performance. **(08 Marks)**

b. Explain the little Endian and the Big Endian addressing scheme. How the message 'MADE' is stored in the memory starting from the address 2000 H using both the schemes. **(08 Marks)**

Module-2

3 a. Explain absolute, indirect, index and autoincrement addressing modes with example. **(06 Marks)**

b. Find the effective address of the memory operand in each of the following instruction:

Load $20(R_1), R_5$
Move #3000, R_5
Store R_5, 30 (R_1, R_2)
Add $-(R_2), R_5$
Subtract $(R_1)+, R_5$

Where $R_1 = 1200$ and $R_2 = 4600$. **(05 Marks)**

c. Explain shift, arithmetic shift and rotate instructions with example. **(05 Marks)**

OR

4 a. Explain the single precision and double precision IEEE standard floating point formats. **(08 Marks)**

b. How the special values 0, ∞ and $\sqrt{-1}$ are represented using single precision IEEE format? **(04 Marks)**

c. Explain PUSH and POP instruction with example. **(04 Marks)**

Module-3

5 a. Explain any two methods of handling multiple devices using interrupt priority schemes. **(08 Marks)**

b. Draw the timing diagram of input data transfer using multiple clock cycles and explain the operation. **(08 Marks)**

OR

6 a. Draw the diagram of DMA controller interface in a computer system and explain the working principle. **(08 Marks)**

b. Draw the timing diagram of PCI bus read operation and explain. **(08 Marks)**

Module-4

7 a. Draw the circuit diagram of SRAM cell and DRAM and explain the read/write operation. **(05 Marks)**

b. Give the list of all possible non-volatile memory. **(03 Marks)**

c. Draw the block diagram of synchronous DRAMs and explain the operation with timing diagram. **(08 Marks)**

OR

8 a. The main memory size is 64 KB and cache memory size is 8 KB. Each memory is divided into the size of 1 KB module. Give the address mapping scheme using (i) direct mapping (ii) associative mapping. **(08 Marks)**

b. Draw the block diagram of virtual memory address translation method and explain how virtual address is converted into the physical address. **(08 Marks)**

Module-5

9 a. Draw the diagram of single-bus organization of the datapath inside a processor and explain the steps to execute an instruction. **(08 Marks)**

b. List the control sequences needed for the execution of an instruction add (R_2), R_1. **(08 Marks)**

OR

10 a. Draw the diagram of three bus organization of the datapath and write the control sequences needed to execute an instruction add R_1, R_2, R_3. **(08 Marks)**

b. Explain with diagram the operation of the microproframmed control unit. **(08 Marks)**

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