CBCS SCHEME

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17MT35

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is filter? Explain its classification? **(04 Marks)**

b. Explain the following :
   i) 3 dB cut-off frequency
   ii) Bandwidth of the filter
   iii) Mid band gain of the filter. **(06 Marks)**

c. Explain the frequency Reponses of High Pass Filter (HPF), Band Pass Filter (BPF) and Band Reject Filter (BRF). Mark the midband gain and width in all the responses. **(10 Marks)**

OR

2 a. Design a first order Butterworth HP filter with cut-off frequency of 1KHz and pass band gain of 2. Plot the frequency response. **(10 Marks)**

b. Design and second order Butterworth LPF at a high cut-off frequency of 2KHz. Plot the frequency response with the mid band gain. **(10 Marks)**

Module-2

3 a. Derive the equations that explain the two criteria required to be fulfilled for oscillator. **(10 Marks)**

b. With a neat circuit diagram, explain phase shift RC oscillator. **(05 Marks)**

c. Design the phase shift oscillator for frequency of oscillation $f_0 = 300Hz$. **(05 Marks)**

OR

4 a. With the help of I/P and O/P waveforms explain the working of zero crossing detector. **(10 Marks)**

b. For Schmitt trigger circuit, explain the following :
   i) Upper Trigger Point (UTP)
   ii) Lower Trigger Point (LTP)
   iii) Plot of Hysteresis Voltage. **(10 Marks)**

Module-3

5 a. List the five features of 555 Timer. **(05 Marks)**

b. With a neat circuit diagram, explain the astable operation of 555 Timer. **(07 Marks)**

c. Explain the architecture of 555 Timer. **(08 Marks)**

OR

6 a. Explain the connection diagram of 555 timer for using it as monstable multi-vibrator. **(08 Marks)**

b. What is the importance of the following pins in 555 timer, when it is used as monostable multi-vibrator.
   i) Trigger Pin (PIN 2) ii) Rest Pin (PIN 4) **(08 Marks)**

c. Explain the operation of 555 Timer as monostable multi-vibration with waveforms. **(04 Marks)**

Module-4

7 a. Explain the full adder circuit with the following :
i) Truth table ii) Logic Diagram. **(10 Marks)**

b. Explain the working of 4 × 1 MUX with operation table, select lines and logic diagram. **(10 Marks)**

OR

8 a. Map the following fucntion on K' map F(A, B, C, D) = ∑1, 5, 6, 9, 14, 15. **(06 Marks)**

b. Impliment the following function using 4 × 1 MUX. F(A, B, C) = ∑1, 3, 5, 7. **(10 Marks)**

c. Draw the K'map for three variables. **(04 Marks)**

Module-5

9 For JK Flip Flop (FF) give the following :

a. Logic diagram
b. Graphic symbol
c. Characteristics table
d. Characteristic equation. **(20 Marks)**

OR

10 a. Design BCD ripple counter with the following details.
i) State diagram ii) Logic diagram iii) Timing diagram. **(10 Marks)**

b. Design synchronous up counter with the following details :
i) Count sequence ii) Logic diagram iii) Input equation for each flip-flop. **(10 Marks)**

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